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# Preparation of Nanoporous Silicon

**by Wayne A. Churaman and Luke Currano**

**ARL-TR-4306** **October 2007**

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**Sensors and Electron Devices Directorate, ARL**

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While research has focused on the optical properties of nanoporous silicon and its use as an isolation material in integrated circuits, there is a great deal to be gained by understanding the formation process of such a versatile material. The structure itself is made up of millions of pores that are formed through an electrochemical wet etch, which results in network clusters of nanoporous material with a surface area on the order of 50 $m^2/g$. In this report, we explore the process of preparing the nanoporous silicon, while presenting solutions to some of the challenges that arise during the pore formation. These challenges include cracking of the nanoporous layer when attempting to etch pores with a vertical depth greater than ~35 μm, as well as effects of electric field concentrations in the etch process, which degrade structural integrity. In addition we provide a quantitative analysis of the material's structural layer and present an alternative approach to the current wet etching technique.

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## Introduction

First discovered by Uhlir in 1957, it was not until the mid-1970's and throughout the 1980's that porous silicon found itself in use as an isolation material in integrated circuits. It then became well known for its photoluminescent properties at room temperature, which was demonstrated by Canham (*1*). These pores are formed through an electrochemical wet-etch process, which can be carried out on both a p-type and n-type silicon substrate. For p-type substrates, the porous material is fabricated in a dark environment to prevent the formation of pores due to the contribution of photogenerated currents (*1*). During the porous etch process, branching networks of nanopores, ranging in vertical depth from a few microns to several hundred microns, are formed. These network clusters of porous silicon have a large surface area; on the order of 30 to 50 $m^2/g$. The ability to attain such large surface area serves as a dominant trait of the material. The porosity of the material is highly dependent on the etch conditions used during the etch process.

Sensors and Electron Devices Directorate has undertaken an effort to explore the science of nanoporous silicon formation in order to further understand the nature of its properties and the dependence on etch parameters. In addition, we seek to understand the structure of the material once it has gone through the electrochemical etch process.

## Nanoporous Silicon Preparation

The nanoporous silicon is formed through an electro-chemical wet etching process, which can be tailored to control the pore depth, as well as (to a lesser extent) the pore size and spacing. Prior to carrying out the electro-chemical etch, the bottom-surface of a boron doped p-type Si wafer is coated with a layer of metal for uniform voltage distribution across the wafer (figure 1a). Double side polished, <100> oriented wafers with a resistivity of 1-30 ohm-cm is the preferred starting material. A Varian 3190 sputter deposition tool is used to deposit a two-metal stack, which includes a 200 Å Ti layer to promote adhesion, followed by an 800 Å Pt layer. Once the wafer has been coated, the silicon substrate is annealed in a rapid thermal anneal furnace (RTA). Tests show that annealing the wafer at 700 ºC for 60 seconds allows for an increased reaction rate between the HF etching solution and the Si substrate. The contact resistance between the metal and the silicon is reduced, allowing more current to flow through the etching solution.

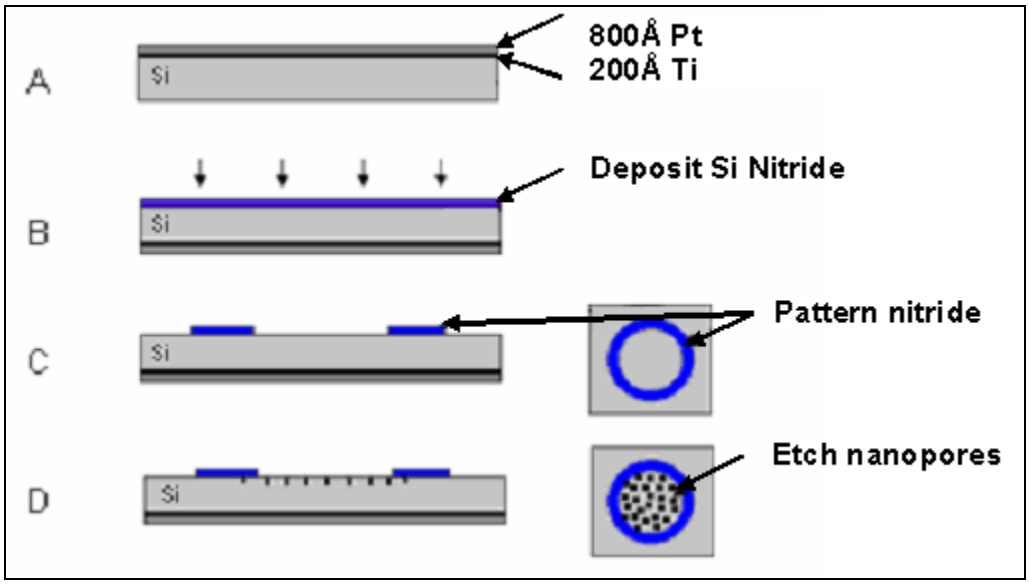


Figure 1. Process flow for nanoporous silicon preparation.

Etching is done in a cylindrical telfon chamber because of the aggressive nature of the hydrofluoric acid used during the etch. The chamber consists of an upper and a lower plate (figure 2), and the wafer is positioned between the two plates. The upper plate contains an open cavity in the center to hold the etchant and is fitted with an o-ring to prevent the etching solution from leaking (figure 3). The lower plate is solid except for screw holes to fasten the two plates together. The etchant used is a solution consisting of a 1:1 mixture of 49% hydrofluoric acid and ethanol. Three different chambers have been designed in order to accommodate various sample sizes, with diameters ranging from 1 cm to 3 ½ inches. The chamber depth remains constant from one chamber design to the next. The smallest chamber holds approximately 3 mL of the etchant solution. Before the chamber can be filled with the etchant, the platinum-coated surface of the Si wafer is placed on top of a small strip of aluminum foil situated on the lower plate of the teflon chamber. This serves as a contact to the Pt anode for the electro-chemical etch process. The upper plate (with the o-ring in place) is fastened to the lower plate and the chamber is filled with the HF and ethanol solution. A gold cathode, suspended from an insulated arm above the chamber is submerged in the liquid etchant (figure 4). A Keithley Model 2400 digital sourcemeter is then connected across the cathode and anode in order to transmit current through the solution and the surface of the Si wafer. The direction of current flow is important; if the connections are switched, no pore formation takes place.

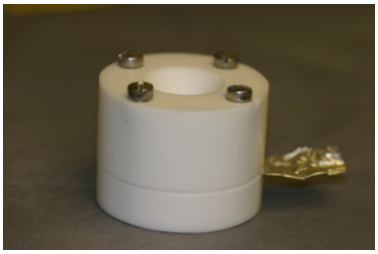

Figure 2. Teflon etch chamber with aluminum foil contacting back electrode.

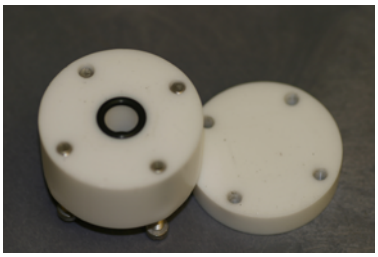

Figure 3. Rubber o-ring seals HF and ethanol solution inside vessel.

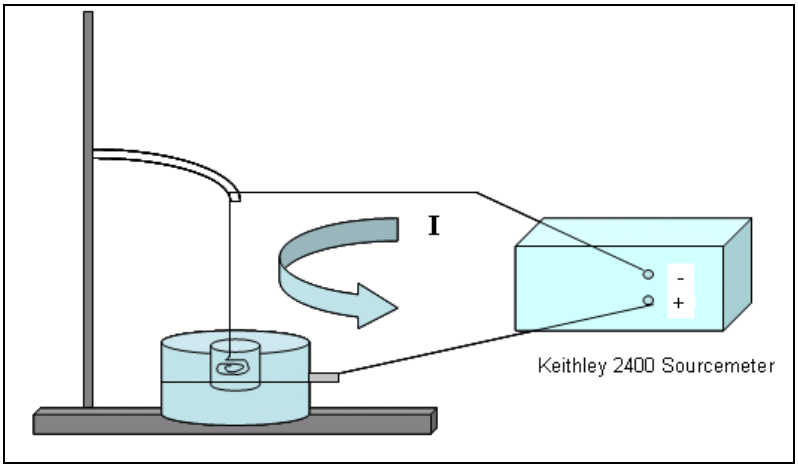


Figure 4. Illustration of etching setup indicating current flow through the sample.

The power supply is set to source a specific amount of current depending on the desired characteristics of the nanoporous layer. As current is passed between the etchant and the Si substrate, the HF solution reacts with the top layer of Si, to form $SiF_4$, which comes out of the solution as a gas (*2*). The second layer of Si begins to form bonds with the hydrogen atoms present in the solution. There are potentially two methods in which the hydrofluoric acid is inserted into the Si-Si bonds. The first method involves the attachment of fluorine from the HF to the surface Si with hydrogen attaching to the underlying Si. As mentioned above, this leaves behind a surface that is hydrogen terminated (*2*). The second type of attack involves the HF oriented in such a way that the hydrogen bonds with surface silicon. This leads to a fluorine

terminated surface, leaving the same morphology as before therefore fostering a continuous etch process (*2*). There are competing theories as to the reason, but if the current density is below a critical level, distinct pores are formed instead of a uniform unetched surface known as electropolishing (figure 1d). Once the etch has been completed the sample is dried in a nitrogen stream.

Preliminary studies show that initial vertical pore depths of 30-50 microns can be achieved at an etch current of 20 $mA/cm^2$ over an etch time of 30 minutes. Deeper etches require tapering the current over time in order to maintain the structural integrity of the nanoporous layer. The pores tend to undergo a branching effect as the depth increases, and the nanoporous layer is also under tensile stress during and after formation. Without carefully decreasing the current as the pores get deeper, the branches eventually meet up with neighboring pores, and combined with the tensile stress, this causes the nanoporous layer to flake and break apart from the sample (figure 5).

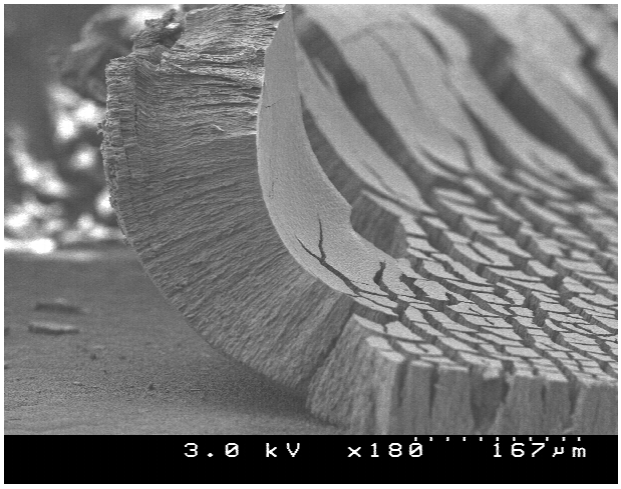


Figure 5. Sample etched a 60$mA/cm^2$ for 1 hour showing visible signs of surface cracking and flaking.

## Pore Analysis

Nanoporous layers can range in thickness from several microns to more than 420 microns based on the etch parameters set by the Keithley source meter. The following SEM images (figures 6 and 7) illustrate the pore structures from a side profile, as well as the tendency of the pores to crack and form branched networks as a result of increased current density. As noted above, structural cracking can be controlled by decreasing the etch current over time. Structural cracking is less likely to occur in thin porous layers (less than 50 μm), but is a critical issue for very thick layers.

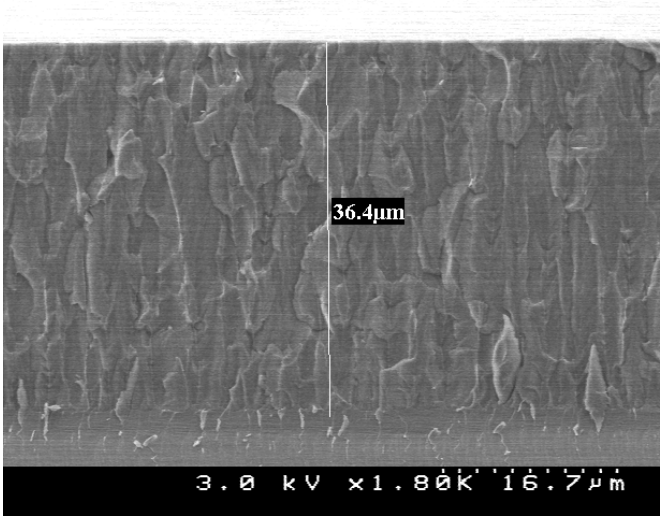


Figure 6. Porous etch at 15 mA/cm$^2$ for 45 minutes.

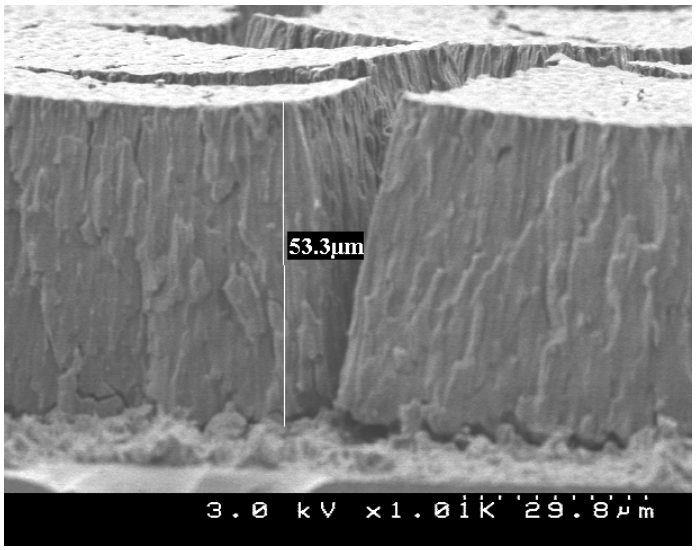


Figure 7. Porous etch at 25 mA for 45 minutes. Formation of clusters can be seen.

For etches deeper than 50 µm, we also noted a tendency for the edge of the sample to etch much faster than the center, which becomes a problem when a deep etch is required (figure 8). The faster etch around the edge produces a trench, which causes the nanoporous layer to detach from the silicon substrate, drastically reducing the surface area and the amount of porous material present. In order to avoid structural cracking, we set up our electro-chemical etch recipe to run for 30 minutes at an etch current of 25 mA, ensuring that our porous layer is approximately 40 µm in vertical depth. Figure 9 shows a plot of the porous etch depth as a function of the etch current over a 30 minute etch time.

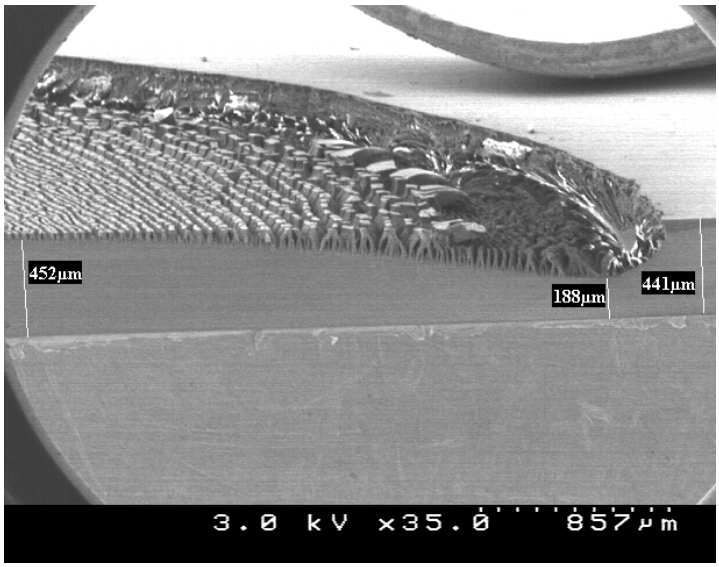


Figure 8. Sample etched at 80 mA for 1 hour. Right corner of the sample has etched much faster than the center, causing the porous layer to break apart.

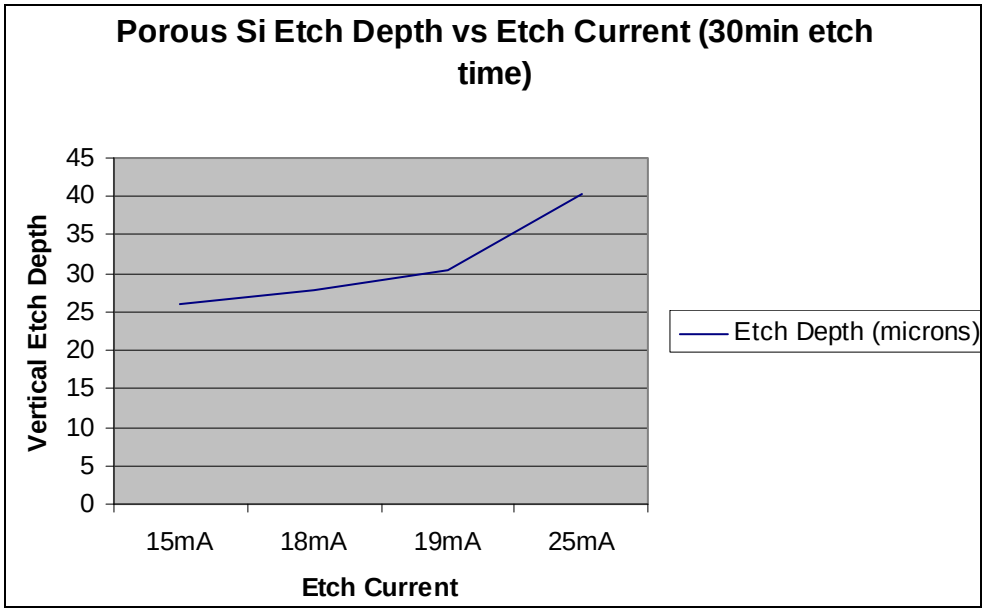


Figure 9. Porous silicon etch depth as a function of etch current.

To study the cause of this over etch, we built a finite element model of the etch cell, including the o-ring, the Teflon chamber, and the etch solution (figure 10). An analysis of the model shows significant electric field concentrations due to the low-permittivity o-ring, which we believe are causing the increased etch rate near the edge. To counteract this effect for longer etches, we mask a portion of the silicon very near the o-ring (1-2 mm from the edge of the o-ring) with a thin layer of PECVD silicon nitride (figures 1b and 1c), which has a higher resistance and

protects the edges from etching at such a fast rate. For shallow etches (less than ~30 μm) this can be ignored with no ill effects.

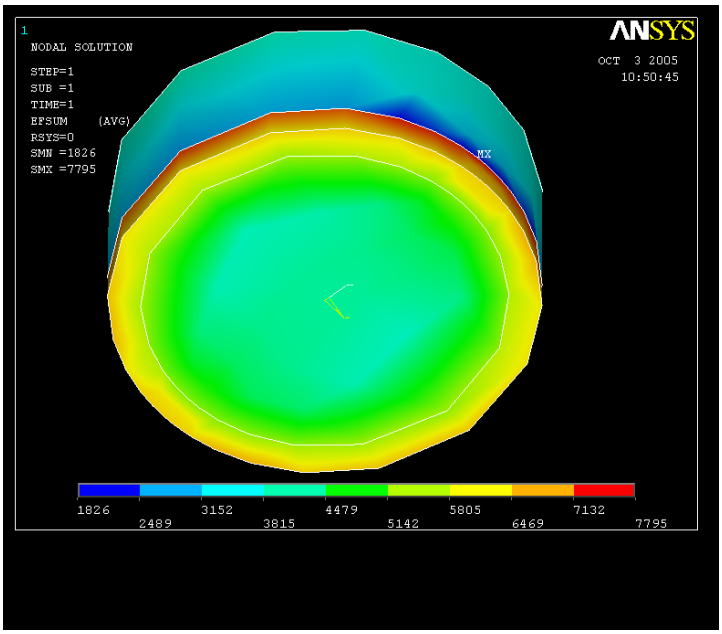


Figure 10. Finite element analysis shows electric field concentration at the edge of the sample due to the o-ring seal.

Analysis has been performed at Aberdeen Proving Ground to gain a better understanding of the structural properties of nanoporous silicon. BET analysis of the pore volume in relation to the pore depth indicates that the average pore diameter is approximately 4.8nm at a pore volume of 0.038 $cm^3$/g-nm (figure 11). This data is based on a 156 minute etch at 375 mA. Etch conditions for the BET analysis were scaled up to account for a circular nanoporous layer 3.5 inches in diameter. As noted above, the pore depth can be controlled by the etch conditions, including sample resistivity, HF and ethanol concentration, and current level. The samples evaluated at the varied etch conditions showed no significant variation in pore diameter. The surface area did show a dependence on etch current (more specifically, the product of etch current and etch time), as shown in figure 12. The larger the total charge which is passed through the wafer, the larger the surface area, which results from deeper or more tightly spaced pores.

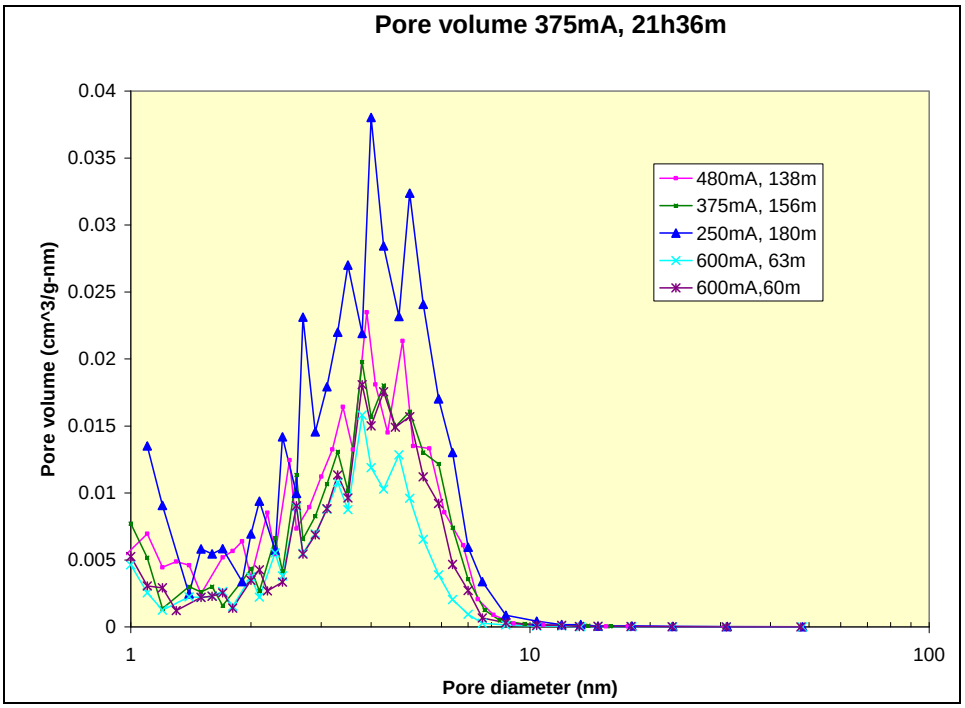


Figure 11. BET analysis of the pore diameter and volume at varied etch conditions.

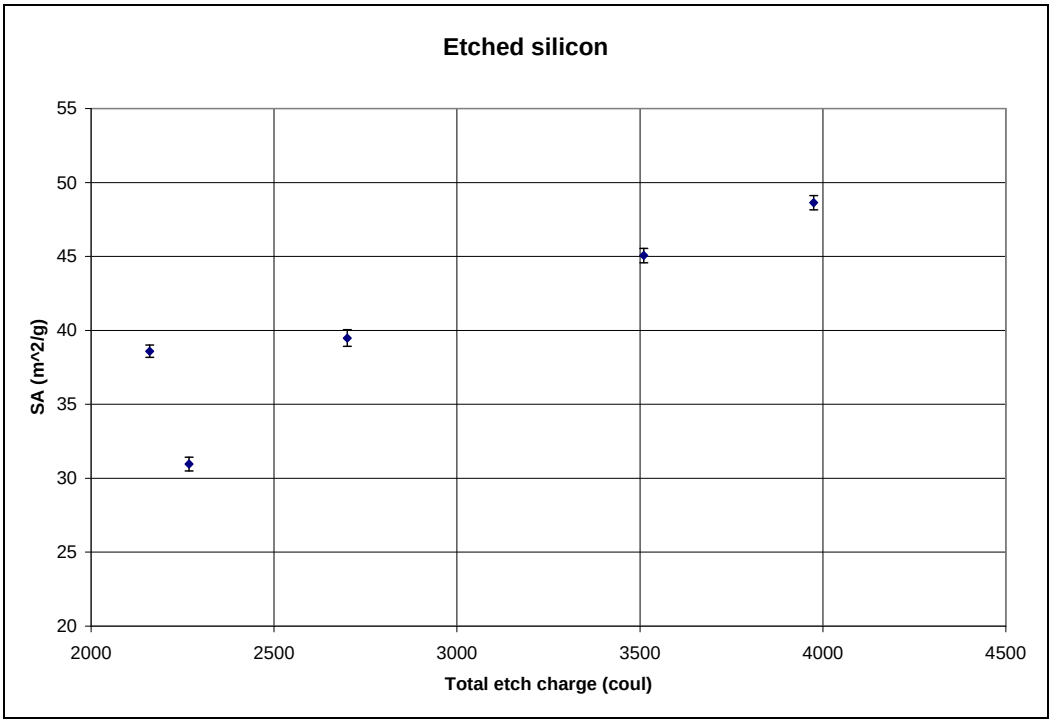


Figure 12. Dependence of total surface area on total etch charge (current x time).

TEM images were taken of the nanoporous material to confirm the pore diameter and to look at the nano-structure of the material. From these images, figure 13, we are able to distinctly see a difference between an individual pore and the surrounding silicon crystalline structure.

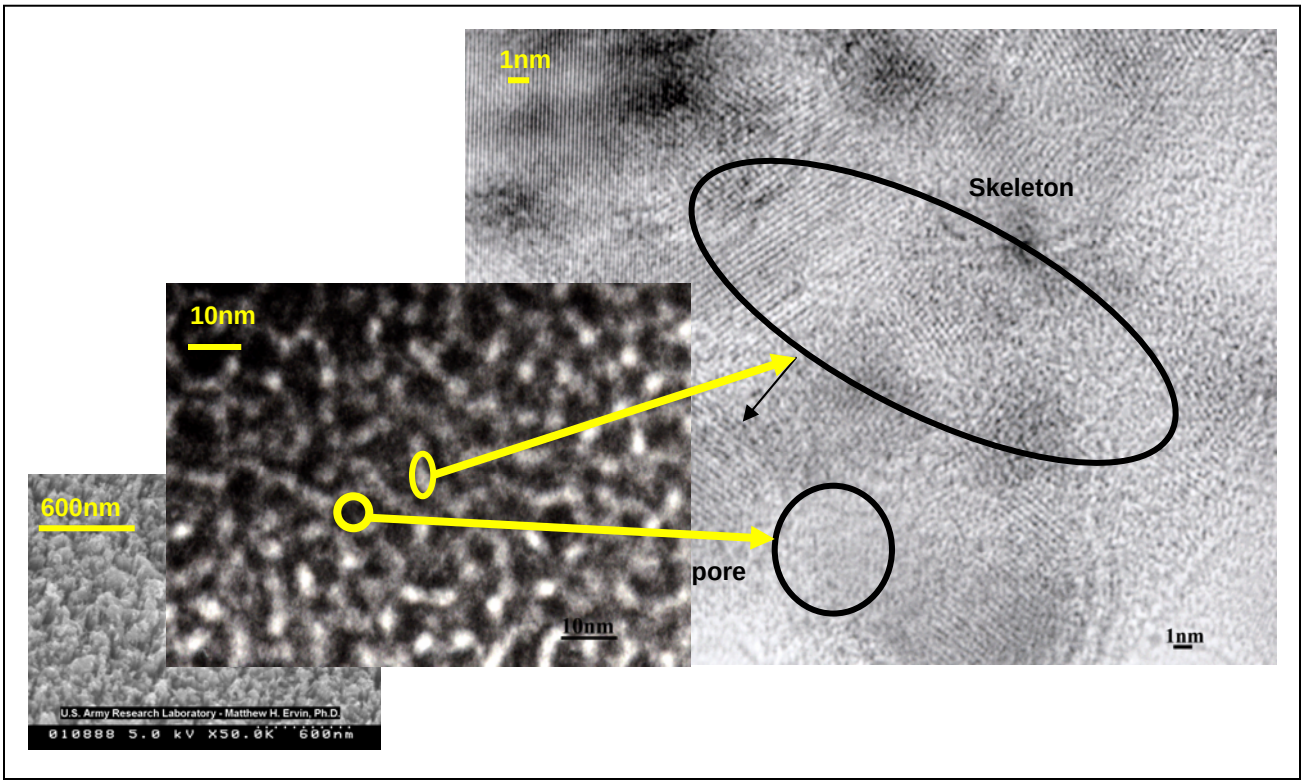


Figure 13. TEM of porous silicon showing individual pore surrounded by crystalline silicon skeletal structure.

## Porous Alumina Template

The present technique used to make nanoporous silicon involves a wet etching process that is both messy and extremely dangerous due to the nature of hydrofluoric acid used in the etching solution. In understanding and studying nanoporous silicon, our goal has also focused on the exploration of new alternatives to etching nanoporous silicon that are both highly effective in achieving adjustable pore depth and avoiding the need for an etchant that requires the use of hydrofluoric acid. In a collaborative effort, the U.S. Army Research Laboratory (ARL) has been working with nanoporous alumina templates that have been developed by Professor Latika Menon at Northeastern University. The porous alumina is formed by an anodization process that involves submersion of an aluminum substrate in an acidic solution with the application of voltage ranging from 5-70 V. During the three step process, oxide dissolution by H+ ions first takes place. This results in the movement of oxide and Al ions through the barrier oxide. Oxide

is then formed at the oxide-Al interface and the electrolyte interface (*3*). Figure 14 is an image of the template that is formed, and its application to a silicon substrate to generate nanopore arrays. The spacing between adjacent pores can be tailored anywhere from 10 nm up to 150 nm, with the thickness of the porous alumina template on the order of several mm.

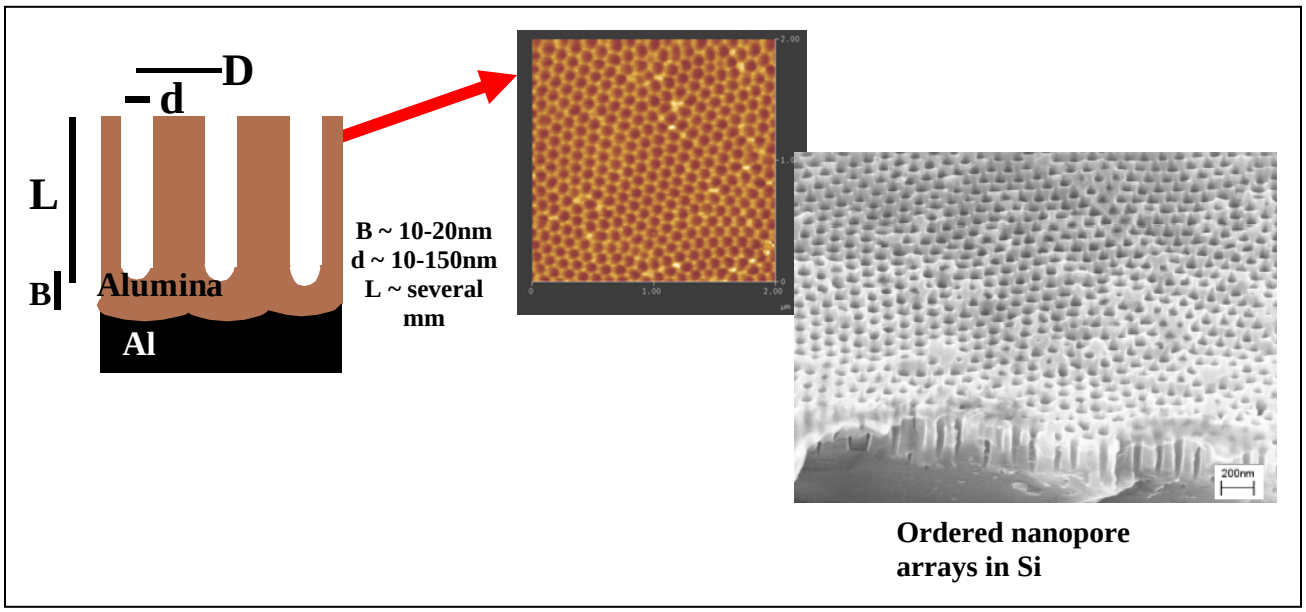


Figure 14. Porous alumina template developed at Northeastern University.

The template can be easily reused and transferred from one substrate to another by moistening its surface with isopropanol and manually repositioning with a pair of fine tweezers. In order to adapt the alumina template to our nanoporous fabrication process, we place the template onto a silicon wafer and carry out a deep reactive ion etch (DRIE) with the template in place. Our initial results indicate that we are able to etch through the template, with the biggest challenge still being to match the etch depth capabilities of the hydrofluoric-ethanol electrolytic solution. With the present DRIE technique incorporating the template, the nanoporous silicon is approximately 5 microns in vertical depth with limitations arising due to the isotropic nature of the DRIE. The pores that are formed begin to undercut the alumina template thus limiting the vertical depth. Figure 15 is a first attempt SEM to fabricate nanoporous silicon using the porous alumina template.

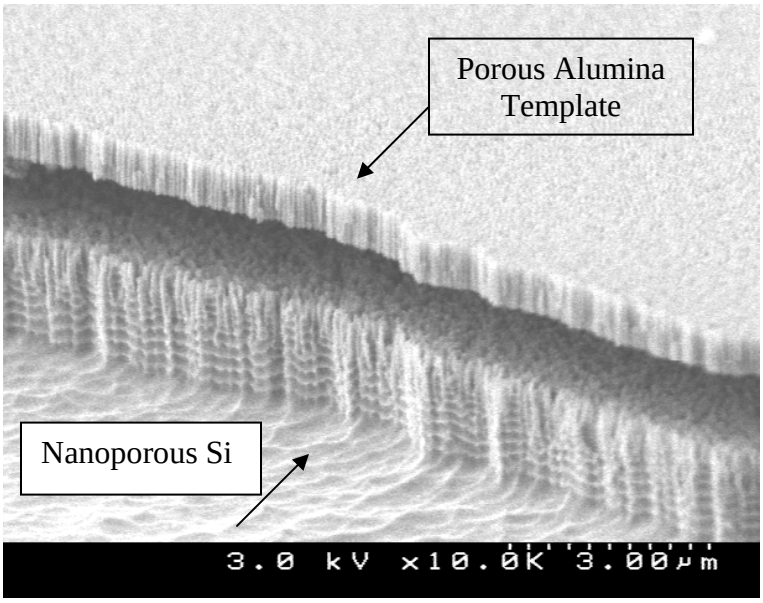


Figure 15. Nanoporous silicon etched using porous alumina template.

## Conclusions

While a great deal has been accomplished by ARL in understanding the science behind the preparation and structural analysis of nanoporous silicon, efforts continue in the development of new alternatives to fabricate this material. While the present fabrication process requires a wet etching technique, we continue to move closer to an adaptable dry etching process that will allow our nanoporous material to be easily integrated into existing MEMS process techniques. Because of the variability in the etch parameters, the structural characteristics of the nanoporous silicon can be readily tailored in order for the material to serve multiple uses.

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2. Trucks, G. W.; Raghavachari, Krishnan; Higashi, G. S.; Chabal, Y. J. Mechanism of HF Etching of Silicon Surfaces: A Theoretical Understanding of Hydrogen Passivation. *Physical Review Letters* **23 July 1990**, *65* (4), AT&T Bell Laboratories, Murray Hill, NJ, 07974.
3. Professor Latika Menon. Northeastern University. Porous Alumina Template Presentation.

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